



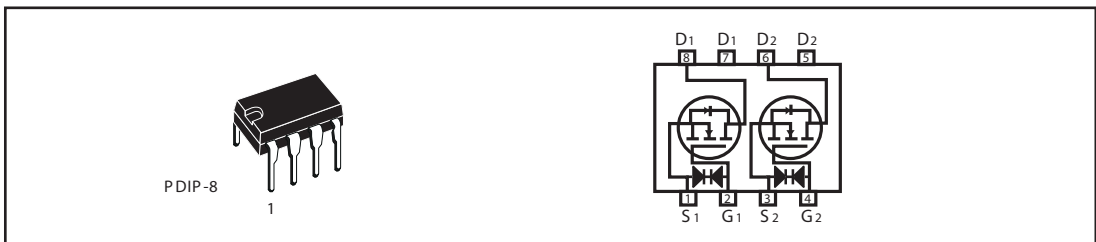
# STA6968

## Dual N-Channel Enhancement Mode Field Effect Transistor

PRODUCT SUMMARY		
V <sub>DSS</sub>	I <sub>D</sub>	R <sub>DS(ON)</sub> ( mΩ ) Max
60V	5.3A	60 @ V <sub>GS</sub> = 10V 70 @ V <sub>GS</sub> = 4.5V

### FEATURES

- Super high dense cell design for low R<sub>DS(ON)</sub>.
- Rugged and reliable.
- Surface Mount Package.
- ESD Protected.



### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub>=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V <sub>DS</sub>	60	V	
Gate-Source Voltage	V <sub>GS</sub>	±20	V	
Drain Current-Continuous <sup>a</sup> @ T <sub>a</sub>	I <sub>D</sub>	25°C	5.3	A
		70°C	4.5	A
-Pulsed <sup>b</sup>	I <sub>DM</sub>	25	A	
Drain-Source Diode Forward Current <sup>a</sup>	I <sub>S</sub>	1.7	A	
Maximum Power Dissipation <sup>a</sup>	P <sub>D</sub>	T <sub>a</sub> =25°C	3	W
		T <sub>a</sub> =70°C	2	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to 150	°C	

### THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient <sup>a</sup>	R <sub>θJA</sub>	41.5	°C/W
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ELECTRICAL CHARACTERISTICS (T<sub>A</sub> 25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ <sup>c</sup>	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250uA	60			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 48V, V <sub>GS</sub> = 0V			1	uA
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V			±10	uA
<b>ON CHARACTERISTICS<sup>b</sup></b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250uA	1.0	1.7	3	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 4.5A		49	60	m ohm
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 3A		55	70	m ohm
On-State Drain Current	I <sub>D(ON)</sub>	V <sub>DS</sub> = 5V, V <sub>GS</sub> = 10V	20			A
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 4.5V, I <sub>D</sub> = 4.5A		13		S
<b>DYNAMIC CHARACTERISTICS<sup>c</sup></b>						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0V f = 1.0MHz		685		pF
Output Capacitance	C <sub>OSS</sub>			85		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			50		pF
Gate resistance	R <sub>g</sub>	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V, f = 1.0MHz		2		ohm
<b>SWITCHING CHARACTERISTICS<sup>c</sup></b>						
Turn-On Delay Time	t <sub>D(ON)</sub>	V <sub>DD</sub> = 30V I <sub>D</sub> = 4.5 A V <sub>GS</sub> = 10V R <sub>GEN</sub> = 6 ohm		11		ns
Rise Time	t <sub>r</sub>			12		ns
Turn-Off Delay Time	t <sub>D(OFF)</sub>			38		ns
Fall Time	t <sub>f</sub>			8		ns
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 48V, I <sub>D</sub> = 4.5A, V <sub>GS</sub> = 10V		12.7		nC
		V <sub>DS</sub> = 48V, I <sub>D</sub> = 4.5A, V <sub>GS</sub> = 4.5V		6.9		nC
Gate-Source Charge	Q <sub>gs</sub>	V <sub>DS</sub> = 48V, I <sub>D</sub> = 4.5 A		1.8		nC
Gate-Drain Charge	Q <sub>gd</sub>	V <sub>GS</sub> = 10V		3.6		nC

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## ELECTRICAL CHARACTERISTICS ( $T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ <sup>c</sup>	Max	Unit
<b>DRAIN-SOURCE DIODE CHARACTERISTICS<sup>b</sup></b>						
Diode Forward Voltage	$V_{SD}$	$V_{GS} = 0V, I_S = 1.7A$		0.8	1.2	V

### Notes

- a. Surface Mounted on FR4 Board,  $t \leq 10\text{sec}$ .
- b. Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
- c. Guaranteed by design, not subject to production testing.

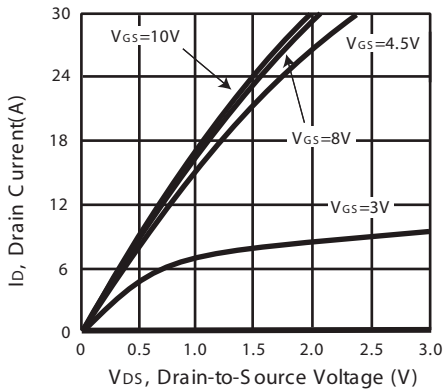


Figure 1. Output Characteristics

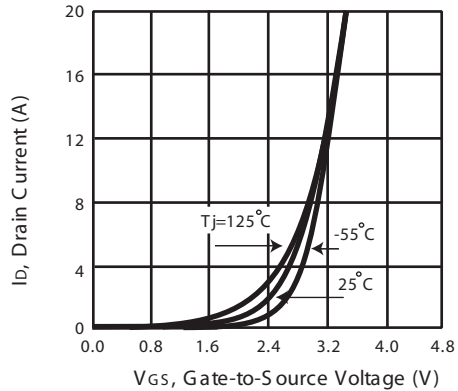


Figure 2. Transfer Characteristics

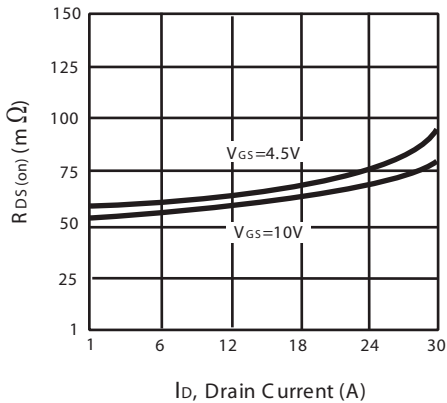


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

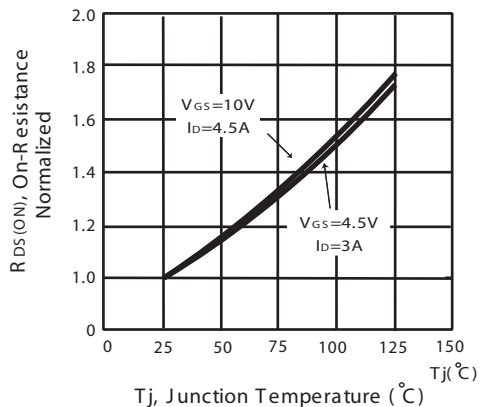


Figure 4. On-Resistance Variation with Drain Current and Temperature

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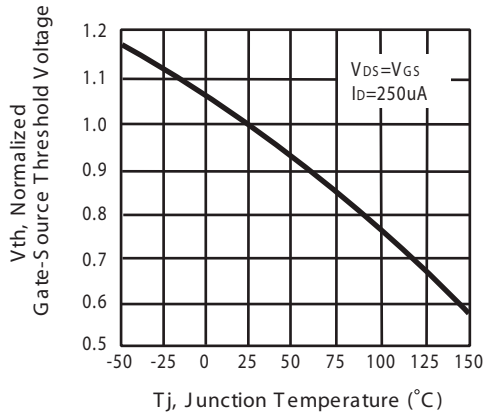


Figure 5. Gate Threshold Variation with Temperature

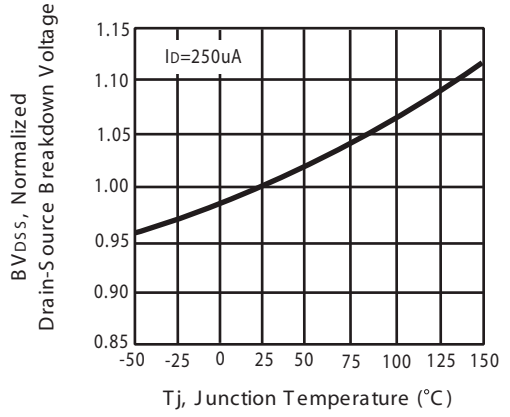


Figure 6. Breakdown Voltage Variation with Temperature

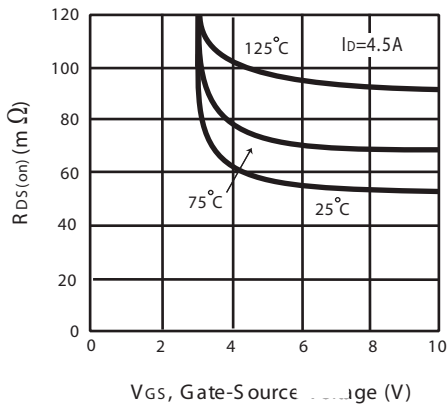


Figure 7. On-Resistance vs. Gate-Source Voltage

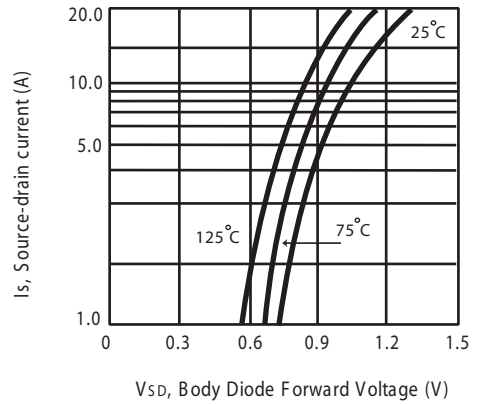


Figure 8. Body Diode Forward Voltage Variation with Source Current

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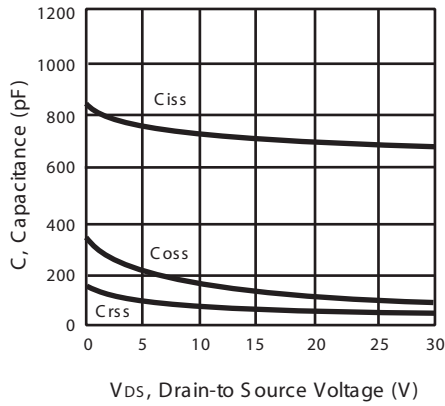


Figure 9. Capacitance

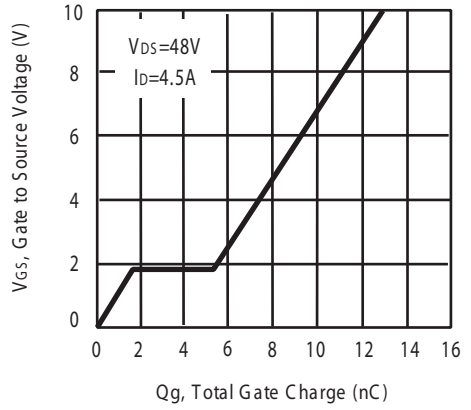


Figure 10. Gate Charge

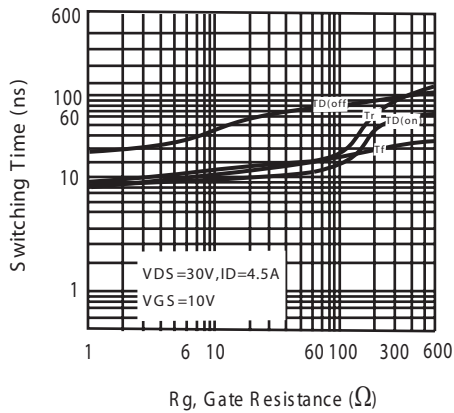


Figure 11. switching characteristics

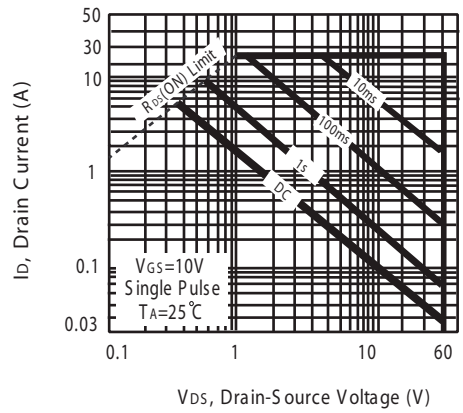
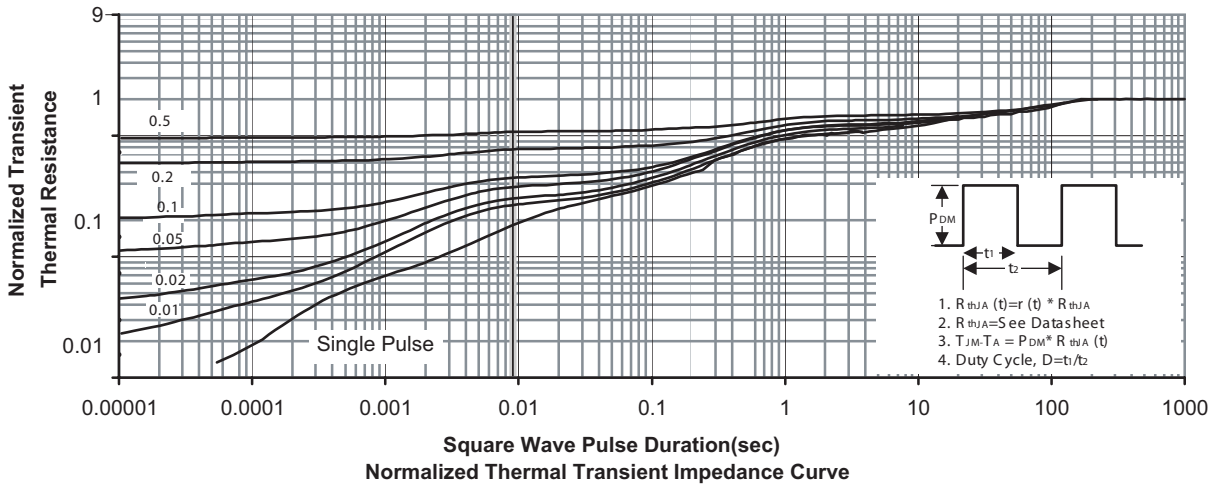


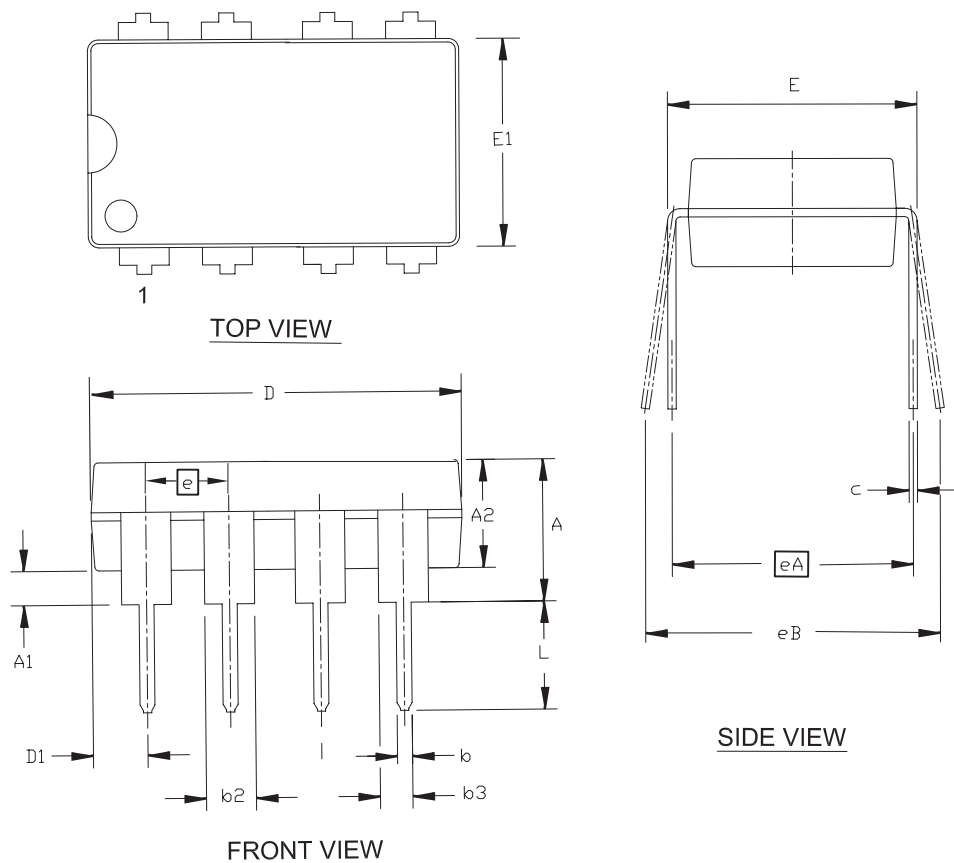
Figure 12. Maximum Safe Operating Area



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## PACKAGE OUTLINE DIMENSIONS

### PDIP 8



SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.145	.172	.200	3.68	4.37	5.08
A1	.020	-	-	0.51	-	-
A2	.125	.130	.135	3.18	3.30	3.43
b	.015	.018	.021	0.38	0.46	0.53
c	.009	.012	.014	0.23	0.30	0.36
b2	.045	.060	.070	1.14	1.52	1.78
b3	.030	.039	.045	0.76	0.99	1.14
L	.125	.132	.140	3.18	3.35	3.56
e	.090	.100	.110	2.29	2.54	2.79
D	.373	.386	.400	9.47	9.80	10.16
D1	.030	.045	.060	0.76	1.14	1.52
E	.300	.310	.320	7.62	7.87	8.13
E1	.245	.250	.255	6.22	6.35	6.48
eA	.280	-	-	7.11	-	-
eB	.310	.325	.365	7.87	8.26	9.27